REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on August 22, 202, and the references cited therewith.

Claims 6-9, 11, 15, and 18-21 are amended, as a result, claims 1, 2, and 4-32 are now pending in this application.

§103 Rejection of the Claims

Claims 1-32 were rejected under 35 USC § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,145,069).

Claim 3 was canceled in the previous amendment and response dated 6-13-02. However, in the office action mailed 8-22-02, Applicant notices that claim 3 is still being considered. Applicant requests that claim 3 be removed from consideration in future office actions.

Regarding claims 1, 2, and 4-32, Applicant respectfully traverses the rejections.

Claims 6-9, 11, 15, and 18-21 are amended to further define the claims. The claims of the present invention recite a memory device comprising a volatile main memory (static and dynamic). The claims of the present invention also recite a compression/decompression engine. The memory device uses the compression/decompression engine to compress data and stores the compressed data into the volatile main memory. The claims of the present invention further recite that all components of the memory device are located in a single chip.

The Dye patent discloses a system having flash memory (non-volatile) memory and a compression/decompression engine. The flash memory is located in one chip. The compression/ decompression engine is located on a separate chip.

Volatile memory and flash memory are two different types of memory.

Because the volatile main memory of the claims of the present invention is different from the flash memory of the system of the Dye patent, and because the single chip feature of present invention is different from the separate chip feature of the Dye patents, Applicant believes that the combination of the volatile main memory feature and the single chip feature of the claims of the invention is novel and not obvious over the Dye patent.

Since Applicant believes claims of the present invention are not obvious, the obviousness rejections stated in Office Action rely on the Applicant's disclosure. The teaching or suggestion to make the claimed element must be found the prior art, not in Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The obviousness rejection must avoid hindsight analysis. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Accordingly, Applicant requests that the rejections of claims 1, 2, and 4-32 be reconsidered and withdrawn and that these claims be allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

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Amy J. Moriarty

Nov. 6, 2002
Date of Transmission

Docket No. 303.663US1
WD # 435830

Micron Ref. No. 99-0510

Clean Version of Pending Claims

HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY
Applicant: Eugene H. Cloud
Serial No.: 09/518,338

Claims 1, 2, 4-32, as of November 6, 2002 (Date Response to Final Office Action filed).

Sub C1 B1

1. A memory device comprising:

a volatile main memory;

a cache memory connected to the volatile main memory; and

a compression and decompression engine connected between the volatile main memory and the cache memory, wherein the volatile main memory, the cache memory, and the compression and decompression engine are located in a single chip.

2. The memory device of claim 1 further comprising, on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.

Sub C1 B2

4. A memory device comprising:

a dynamic memory;

a static memory connected to the dynamic memory;

a compression and decompression engine connected between the dynamic memory and the static memory; and

an error detection and correction engine connected to the dynamic memory and the compression and decompression engine, wherein the dynamic memory, the static memory, the compression and decompression engine, and the error detection and correction engine are located in a single chip.

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Sub C1 B2

5. The memory device of claim 4 wherein the error detection and correction engine is connected between the dynamic memory and the compression and decompression engine.

6. (Amended) A memory device comprising:

an input/output buffer;

a cache memory connected to the input/output buffer;

a compression and decompression engine connected to the cache memory; and

a volatile main memory connected to the compression and decompression engine, wherein the input/output buffer, the cache memory, the compression and decompression engine, and the volatile main memory and are located in a single chip.

7. (Amended) The memory device of claim 6 wherein the compression and decompression engine is connected between the volatile main memory and the cache memory.

8. (Amended) The memory device of claim 7 further comprising ,on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.

9. (Amended) A system comprising:

a processor; and

a memory device connected to the processor, the memory device comprising a volatile main memory and a compression and decompression engine connected to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

10. The system of claim 9 wherein the memory device further comprises ,on the single chip, an error detection correction engine connected to the compression and decompression engine.

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11. (Amended) A system comprising:

a processor; and

a memory device connected to the processor, wherein the memory device comprises a volatile main memory, a compression and decompression engine connected to the volatile main memory , and a cache memory connected to the compression and decompression engine, wherein the volatile main memory, the compression and decompression engine, and the cache memory and are located in a single chip.

12. The system of claim 11 wherein the memory device further comprises ,on the single chip, an error detection correction engine connected to the compression and decompression engine.

13. The system of claim 11 further comprising a graphic control card, wherein the graphic control card connects to the memory device.

14. The system of claim 11 further comprising a video control card, wherein the video control card connects to the memory device.

15. (Amended) A method of increasing a storage density of a memory device, the method comprising:

providing a volatile main memory;

providing a compression and decompression engine; and

connecting the compression and decompression engine to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

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16. The method of claim 15 further comprising:
providing a cache memory in the single chip; and
connecting the cache memory to the compression and decompression engine.

17. The method of claim 15 further comprising:
providing an error detection and correction engine in the single chip; and
connecting the error detection and correction engine to the compression and decompression engine.

18. (Amended) A method of operating a memory device, comprising:
receiving input data at a cache memory;
compressing the input data at a compression and decompression engine to produce compressed data; and
storing the compressed data into a volatile main memory, wherein the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

19. (Amended) The method of claim 18 further comprising:
reading the compressed data from the volatile main memory;
decompressing the compressed data at the compression and decompression engine to produced decompressed data; and
reading the decompressed data to the cache memory.

20. (Amended) A method of operating a memory device, comprising:
receiving data at an input/output buffer;
processing the data at a cache memory to produce processed data;
compressing the processed data at a compression and decompression engine to produce

compressed data; and

storing the compressed data into a volatile main memory , wherein the input/output buffer, the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

21. (Amended) The method of claim 20 further comprising:

reading the compressed data from the volatile main memory;

decompressing the compressed data at the compression and decompression engine to produced decompressed data;

reading the decompressed data at the cache memory; and

transferring the data to the input/output buffer.

22. A memory device comprising:

an input/output buffer;

a static memory connected to the input/output buffer;

a compression and decompression engine connected to the static memory; and

a dynamic memory connected to the compression and decompression engine, wherein the input/output buffer, the static memory, the compression and decompression engine, and the dynamic memory and are located in a single chip.

23. The memory device of claim 22 further comprising, on the single chip, an error detection and correction engine connected to the dynamic memory and the compression and decompression engine.

24. A system comprising:

a processor; and

a dynamic random access memory device connected to the processor, the dynamic

Sub C1

random access memory device including a plurality of memory blocks and a compression and decompression engine connected to the memory blocks, wherein the memory blocks and the compression and decompression engine are located in a single chip.

25. The system of claim 24 wherein the memory device further comprises, on the single chip, an error detection correction engine connected to the compression and decompression engine.

26. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of dynamic memory blocks;

a compression and decompression engine connected to the dynamic memory blocks;

and a static memory block connected to the compression and decompression engine;

and

an error detection correction engine connected to the compression and decompression engine, wherein the dynamic memory blocks, the compression and decompression engine, the static memory block, and the error detection correction engine are located in a single chip.

27. The system of claim 26 further comprising a graphic control card connected to the memory device.

28. The system of claim 27 further comprising a video control card connected to the memory device.

29. A method of operating on data comprising:

receiving input data;

compressing the input data to produce compressed data;

storing the compressed data;

reading the compressed data; and

decompressing the compressed data, wherein receiving, compressing, storing, reading, and decompressing are performed on a single chip.

30. The method of claim 29 further comprising:

detecting for an error during compressing and decompressing; and

correcting the error during compressing and decompressing.

31. A method of operating on data comprising:

receiving input data at a static memory block;

compressing the input data to produce compressed data;

storing the compressed data into a dynamic memory block;

reading the compressed data from the dynamic memory block; and

decompressing the compressed data, wherein receiving, compressing, storing, reading, and decompressing are performed on a single chip.

32. The method of claim 31 further comprising:

detecting for an error during compressing and decompressing; and

correcting the error during compressing and decompressing.